ABSTRACT

A semiconductor memory includes a memory cell array, a redundancy repair signal generator, and a row decoder. The memory cell array includes a plurality of memory cell rows and at least one redundant memory cell row. The redundancy repair signal generator generates a redundancy repair signal that indicates an address of a defective memory cell row. The row decoder receives a row address signal that indicates a memory cell row including a memory cell to be accessed and selects the redundant memory cell row in accordance with the redundancy repair signal generated by the redundancy repair signal generator. The redundancy repair signal generator is located opposite to the row decoder with the memory cell array placed therebetween. This configuration can achieve a reduction in free space and thus a reduction in area loss.